In the Claims:

Please cancel claims 12-19. Please amend claims 1-7 and 9-11. Please add new claims 20-28. The claims are as follows:

1. (Currently Amended) A capacitor formed on a substrate, comprising:

a ~~single-crystal~~ Fin structure having a top surface and a first side surface opposite a second side surface, said Fin structure including a single-crystal semiconductor material;

an insulator structure adjacent the top surface of the ~~at least one~~ Fin structure; and

a conductor structure adjacent the ~~at least one~~ insulator structure ~~over a portion of the at least one Fin structure~~, wherein the conductor structure partially but not totally overlays the Fin structure, and wherein a thickness of the conductor structure is within a thickness of the Fin structure, said thickness of the Fin structure being a distance between the first and second side surfaces of the Fin structure , said thickness of the conductor structure being oriented in a same direction as said thickness of the Fin structure, said insulator structure comprising a single insulative material distributed from the top surface of the Fin structure to a bottom surface of the conductor structure.

2. (Currently Amended) The capacitor of claim 1, further comprising ~~at least one~~ a first interconnect ~~disposed adjacent~~ connected to one of the top surface, the first side surface, and the second side surface of the ~~at least one~~ Fin structure.

3. (Currently Amended) The capacitor of claim ~~1~~ 2, further comprising ~~at least one~~ a second interconnect ~~disposed adjacent the at least one~~ connected to the conductor structure.

4. (Currently Amended) The capacitor of claim 1, wherein the ~~at least one~~ conductor structure ~~is~~ includes a conductive material selected from the group consisting of a metal, a metal silicide, and doped polysilicon.

5. (Currently Amended) The capacitor of claim 1, wherein the ~~at least one single-crystal Fin structure has a given width, and wherein the at least one conductor structure partially at least one Fin structure~~ thickness of the Fin structure is greater than 40 nm.

6. (Currently Amended) The capacitor of claim 1, wherein the ~~at least one single-crystal Fin structure is narrow, has a given width and wherein the at least one insulator structure is adjacent both the first side surface and the second side surface of the at least one Fin structure, thereby encapsulating the at least one~~ Fin structure has a height between 10 nm and 160 nm.

7. (Currently Amended) The capacitor of claim ~~6~~ 1, wherein said first single-crystal Fin structure has conductivity-enhancing dopant ions therein.

8. (Original) The capacitor of claim 1, wherein a FinFET is disposed on the substrate, the FinFET having a gate electrode coupled to said conductor structure.

9. (Currently Amended) The capacitor of claim ~~9~~ 1, wherein the ~~substrate comprises a SOI substrate~~ single insulative material is silicon dioxide or silicon nitride.

10. (Currently Amended) An integrated circuit chip, comprising ~~at least one~~ a first nominal-voltage decoupling capacitor and ~~at least one~~ a second high-voltage decoupling capacitor, respectively comprising:

a first ~~single-crystal~~ Fin structure having a first ~~width~~ thickness and a second single-crystal Fin structure having a second ~~width~~ thickness greater than said first ~~width~~ thickness, said first Fin structure and said second Fin structure each having a top surface and a first side surface opposite a second side surface, said first thickness being a distance between the first and second side surfaces of the first Fin structure, said second thickness being a distance between the first and second side surfaces of the second Fin structure, said first Fin structure including a single-crystal semiconductor material, said second Fin structure including the single-crystal semiconductor material;

a first insulator structure adjacent the top surface, the first side surface, and the second side surface of the first Fin structure, thereby encapsulating the first Fin structure, and ~~at least one~~ a second insulator structure adjacent the top surface of the second Fin structure; and

a first conductor structure adjacent the first insulator structure ~~over a portion of the first Fin structure~~, and a second conductor structure adjacent the ~~at least one~~ second insulator structure ~~over a portion of the second Fin structure~~, wherein ~~so that~~ the second conductor structure partially but not totally overlays the second Fin structure and a thickness of the second conductor structure is within a thickness of the second Fin structure, and wherein the first conductor structure totally overlays the first Fin structure and a thickness of the first Fin structure is within a thickness of the first conductor structure, said thickness of the first conductor structure being oriented in a same direction as said thickness of the first Fin structure, said thickness of the

second conductor structure being oriented in a same direction as said thickness of the second Fin structure, said first insulator structure comprising a single insulative material distributed from the top surface of the first Fin structure to a bottom surface of the first conductor structure, said second insulator structure comprising a single insulative material distributed from the top surface of the second Fin structure to a bottom surface of the second conductor structure.

11. (Currently Amended) The integrated circuit chip of claim 10, wherein said second ~~single-crystal~~ Fin structure has conductivity-enhancing dopant ions therein.

12. (Canceled)

13-19. (Canceled)

20. (New) A capacitor formed on a substrate, comprising:

a Fin structure having a top surface and a first side surface opposite a second side surface, said Fin structure including a single-crystal semiconductor material;

an insulator structure adjacent the top surface of the Fin structure; and

a conductor structure adjacent the insulator structure, wherein the conductor structure totally overlays the Fin structure, wherein a thickness of the Fin structure is within a thickness of the conductor structure, said thickness of the Fin structure being a distance between the first and second side surfaces of the Fin structure, said thickness of the conductor structure being oriented in a same direction as said thickness of the Fin structure, said insulator structure comprising a

single insulative material distributed from the top surface of the Fin structure to a bottom surface of the conductor structure.

21. (New) The capacitor of claim 20, further comprising at least one a first interconnect connected to one of the top surface, the first side surface, and the second side surface of the Fin structure.

22. (New) The capacitor of claim 21, further comprising a second interconnect connected to the conductor structure.

23. (New) The capacitor of claim 20, wherein the conductor structure includes a conductive material selected from the group consisting of a metal, a metal silicide, and doped polysilicon.

24. (New) The capacitor of claim 20, wherein the thickness of the Fin structure is in a range of 0.3 nm to 40 nm.

25. (New) The capacitor of claim 20, wherein the Fin structure has a height between 10 nm and 160 nm.

26. (New) The capacitor of claim 20, wherein the single insulative material is silicon dioxide or silicon nitride.

27. (New) The capacitor of claim 20, wherein a FinFET is disposed on the substrate, the FinFET having a gate electrode coupled to said conductor structure.

28. (New) The capacitor of claim 20, wherein the substrate comprises a SOI substrate.